IN THE CLAIMS

1. (Currently Amended) A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

an edge-defined vertical floating gate located above a portion of the channel region and separated from the channel region by a first thickness insulator material;

a first edge-defined vertical control gate located above another portion of the channel region and separated therefrom by a second thickness insulator material, wherein the ~~the~~ first vertical control gate is parallel to and opposing the vertical floating gate on a first side of the vertical floating gate, and wherein the ~~the~~ first vertical control gate is separated from the vertical floating gate by an intergate dielectric;

a second edge-defined vertical control gate located on a second side of the vertical floating gate that is parallel and opposing the vertical floating gate and separated from the vertical floating gate by the ~~integrate~~ intergate dielectric; and

an edge-defined horizontal control gate coupled on its opposing sides to top portions of the first and second vertical control gates and separated from the vertical floating gate by the ~~intergrate~~ intergate dielectric.

2. (Previously Presented) The memory cell of claim 1, wherein at least one of the control gates has a horizontal width of approximately 100 nanometers (nm).

3. (Original) The memory cell of claim 1, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

4. (Original) The memory cell of claim 1, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO2).

5. (Original) The memory cell of claim 1, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

6. (Original) The memory cell of claim 1, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

7. (Previously Presented) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical floating gate separated from a first portion of the channel region by a first oxide thickness;

a first edge-defined vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the first vertical control gate is parallel to and opposing a first side of the vertical floating gate;

a second edge-defined vertical control gate separated from the second portion of the channel region by the second oxide thickness, wherein the second vertical control gate is parallel to and opposing a second side of the vertical floating gate; and

a horizontal edge-defined control gate coupled to top portions of the first and second vertical control gates.

8. (Original) The transistor of claim 7, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

9. (Original) The transistor of claim 7, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

10. (Previously Presented) The transistor of claim 7, wherein the vertical control gates have horizontal widths of approximately 100 Angstroms (Å).

11. (Previously Presented) The transistor of claim 7, wherein the vertical floating gate separated from a first portion of the channel region includes a first portion of the channel region which is adjacent to the source region, and wherein the vertical controls gate separated from ~~a~~ the second portion of the channel region includes a second portion of the channel region which is adjacent to the drain region.

12. (Previously Presented) The transistor of claim 11, wherein the horizontal control gate and the vertical control gates are separated from the vertical floating gate by an intergate dielectric.

13. (Previously Presented) The transistor of claim 7, wherein a capacitance between the control gates and the floating gate is greater than a capacitance between the floating gate and the channel.

14. (Previously Presented) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness;

a third edge-defined vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness; and

a horizontal gate coupled to top portions of the first vertical gate and the third vertical gate and separated from the second vertical gate by an intergate dielectric, and wherein the first

and third vertical gates oppose one another on opposite sides of the second vertical gate and are also separated from the second vertical gate by the intergate dielectric.

15. (Canceled)

16. (Previously Presented) The floating gate transistor of claim 14, wherein the second vertical gate is a floating gate and wherein the second and ~~the~~ third vertical gates and the horizontal gate are control gates.

17. (Previously Presented) The floating gate transistor of claim 14, wherein second vertical gate is a control gate and wherein the second and third vertical gates and the horizontal gate are floating gates.

18. (Canceled)

19. (Previously Presented) The floating gate transistor of claim 14, wherein a greater percentage of a voltage applied to the first and third vertical gates and the horizontal gate appears between the second vertical gate and the channel than between the second vertical gate and the first and third vertical gates and the horizontal gate.

20. (Original) The floating gate transistor of claim 14, wherein the second and the third portion of the channel region are adjacent the source region and the drain region, respectively.

21. (Original) The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO2).

22. (Original) The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate each have a horizontal width of approximately 100 nanometers (nm).

23. (Original) The floating gate transistor of claim 14, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

24-69. (Canceled)

70. (Currently Amended) A memory cell, comprising:

a horizontal gate coupled to top portions of two opposing vertical gates, and wherein the vertical gates are parallel with one another; and

a non-coupled vertical gate separated from the two vertical gates and the horizontal gate by a intergate dielectric, wherein the non-coupled vertical gate separates the two vertical gates.

71. (Previously Presented) The memory cell of claim 70 wherein the horizontal gate and the two vertical gates are control gates and the non-coupled vertical gate is a floating gate.

72. (Previously Presented) The memory cell of claim 70 wherein the horizontal gate and the two vertical gates are floating gates and the non-coupled vertical gate is a control gate.

73. (Previously Presented) A memory cell comprising:

a horizontal floating gate coupled to the ends of two opposing and parallel vertical floating gates; and

a vertical control gate that is separated from the floating gates by an intergate dielectric, and wherein the vertical gate is also parallel to and separates the two parallel vertical gates.

74. (Previously Presented) The memory cell of claim 73 wherein the gates are located above a channel region for the memory cell.

75. (Previously Presented) The memory cell of claim 75 wherein the channel region separates source and drain regions of a horizontal substrate for the memory cell.

76. (Previously Presented) A transistor comprising:

a first control gate;

a second control gate;

a third control gate; and

a floating gate;

wherein the control gates surround the floating gate on three sides of the floating gate and are separated from the control gate by an intergate dielectric, and wherein at least two of the control gates are separated by and parallel to the floating gate.

77. (Previously Presented) The transistor of claim 76 wherein the at least two control gates and the floating gate are vertical gates.

78. (Previously Presented) The transistor of claim 76 wherein the second and third control gates are coupled to the first control gate on their top vertical portions.

79. (Previously Presented) A transistor comprising:

three coupled gates coupled on their ends with one another, where two of the coupled gates are parallel with one another; and

a non-coupled gate surrounded on three sides by the three coupled gates and separating the two parallel gates, and further separated by an intergate dielectric from the three coupled gates.

80. (Previously Presented) The transistor of claim 79 wherein the two parallel gates are coupled indirectly with one another through the remaining coupled gate.

81. (Previously Presented) The transistor of claim 79 wherein the three coupled gates are control gates and the non-coupled gate is a floating gate.

82. (Previously Presented) The transistor of claim 79 wherein the three coupled gates are floating gates and the non-coupled gate is a control gate.